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PATENT APPLICATION

DYNAMICALLY ADJUSTABLE TERMINATION IMPEDANCE CONTROL TECHNIQUES

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DYNAMICALLY ADJUSTABLE TERMINATION IMPEDANCE CONTROL TECHNIQUES

BACKGROUND OF THE INVENTION

[0001] This patent application relates to on-chip impedance termination circuits, and more particularly, to on-chip impedance termination circuits that are programmable and dynamically adjustable.

[0002] Integrated circuits have input/output (IO) pins that are used to transmit signals into and out of the circuit. An external termination resistor can be coupled to each IO pin to provide impedance termination. An impedance termination resistor reduces reflection of input signals on a transmission line coupled to an IO pin. Signal reflection causes signal distortion and degrades overall signal quality. A termination resistor can be selected to match the impedance of a transmission line to eliminate or reduce reflection.

[0003] The use of external resistors for termination purposes can be cumbersome and costly, especially for integrated circuits that have numerous IO pins. For example, external resistors typically use a substantial amount of board space. External resistors also degrade signal quality because of the lumped capacitance associated with physically mounting (or soldering) the resistor on the board. The lumped capacitance doesn't behave as a transmission line and may increase impedance mismatch.

[0004] To address some of the problems with external termination resistors, on-chip impedance termination techniques have been developed. Prior art integrated circuits have provided on-chip impedance termination by coupling an on-chip resistor to an IO pin. The on-chip resistor can be formed from polysilicon. The resistance of an on-chip polysilicon resistor can vary more than 30% across the standard operating temperatures of an integrated circuit (e.g., −5°C to 120°C). Variations in other technology parameters such as supply voltage can also causes substantial variations in the resistance values of on-chip polysilicon termination resistors.

[0005] Another problem with prior art on-chip termination resistors is that their resistance values are fixed. Different IO standards require different termination resistances to match the impedance of different transmission lines.

[0006] Therefore, it would be desirable to provide on-chip impedance termination circuits that can be dynamically adjusted to match the impedance of different transmission lines and varying operating conditions.

BRIEF SUMMARY OF THE INVENTION

[0007] The present invention provides techniques for dynamically adjustable on-chip impedance termination circuits. The present invention allows for real-time adjustment of on-chip programmable termination impedance. For example, a user can build a feedback circuit based on an algorithm programmed into an integrated circuit. The feedback circuit can sense a condition in the integrated circuit (such as temperature) and automatically adjust the on-chip termination impedance in real-time to account for changes in the condition.

[0008] The termination impedance circuits of the present invention include networks of resistors on an integrated circuit that provide termination impedance to transmission lines coupled to IO pins. The termination resistors are coupled in series and in parallel with each other. Pass gates are coupled to the resistors. The pass gates are individually turned ON to couple resistors to the IO pin. The pass gates are individually turned OFF to decouple resistors from the IO pin. Each pass gate is set to be ON or OFF to provide a selected termination resistance value to a transmission line coupled to the IO pin.

[0009] The present invention can also generate different termination resistance values at each IO pin. Also, the termination resistance values can be adjusted to accommodate changes in temperature, voltage, and other factors. The termination resistance values can be increased or decreased to match the impedance of different transmission lines.

[0010] Other objects, features, and advantages of the present invention will become apparent upon consideration of the following detailed description and the accompanying drawings, in which like reference designations represent like features throughout the figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figures 1A-1B are block diagrams of dynamically adjustable impedance termination circuits coupled to output pins on an integrated circuit according to embodiments of the present invention;

[0012] Figures 2A-2B are block diagrams of dynamically adjustable impedance termination circuits coupled to input pins on an integrated circuit according to embodiments of the present invention;

[0013] Figure 3 is a schematic of a dynamically adjustable on-chip termination impedance circuit according to an embodiment of the present invention;

[0014] Figure 4 is a simplified block diagram of a programmable logic device that can implement embodiments of the present invention; and

[0015] Figure 5 is a block diagram of an electronic system that can implement embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0016] Figure 1A illustrates a block diagram of two dynamically adjustable termination impedance circuits 20 on an integrated circuit according to an embodiment of the present invention. An integrated circuit of the present invention can include, for example, an application specific integrated circuit (ASIC), a programmable logic device (PLD), a field programmable gate array (FPGA), a programmable gate array (PLA), or a configurable logic array.

[0017] OUT1 and OUT2 are differential output pins of the integrated circuit. Buffer 10 is a differential driver circuit that drives differential signals out of the integrated circuit and onto transmission lines that are coupled to pins OUT1 and OUT2.

[0018] Termination impedance circuits 20 are coupled together at their common mode (CM) terminals. Termination impedance circuits 20 are coupled to pins OUT1 and OUT2 at their IN terminals. Circuits 20 are coupled in parallel with transmission lines connected to pins OUT1 and OUT2. Thus, circuits 20 provide parallel termination impedance at differential pins OUT1 and OUT2.

[0019] Termination impedance circuit 20 can also provide termination impedance to a single-ended output pin OUT as shown in Figure 1B. In the embodiment of Figure 1B, circuit 20 is coupled between output pin OUT and ground. The IN terminal of circuit 20 is coupled to OUT, and the CM terminal of circuit 20 is coupled to ground. Buffer 30 is a single-ended driver circuit that drives single-ended signals onto a transmission line coupled to

OUT. Circuit 20 provides parallel termination impedance to the transmission line coupled to OUT.

[0020] Termination impedance circuit 20 can also provide termination impedance to input pins as shown in Figures 2A-2B. In Figure 2A, IN1 and IN2 are differential input pins of the integrated circuit. Buffer 70 is a differential driver circuit that drives differential input signals from IN1 and IN2 into the integrated circuit. Termination impedance circuits 20 are coupled in parallel with transmission lines connected to pins IN1 and IN2. Thus, circuits 20 provide parallel termination impedance at differential pins IN1 and IN2.

[0021] In the embodiment of Figure 2B, circuit 20 is coupled between input pin IN and ground. The IN terminal of circuit 20 is coupled to OUT, and the CM terminal of circuit 20 is coupled to ground. Buffer 80 is a single-ended driver circuit that drives single-ended input signals into the integrated circuit. Circuit 20 provides parallel termination impedance to the transmission line coupled to IN.

[0022] Figure 3 illustrates a detailed schematic of dynamically adjustable termination impedance circuit 20 according to an embodiment of the present invention. Termination circuit 20 includes multiple resistor networks 101. Two resistor networks 101 are shown in Figure 3 as an example and to simplify the drawing. Termination circuit 20 can include any number N of resistor networks 101-1 through 101-N. For example, circuit 20 can include 1, 3, 4, 5, 6, 7, or 10 resistor networks 101. Resistor networks 101 are coupled in parallel between the IN and CM terminals of termination impedance circuit 20.

[0023] Each of resistor networks 101 includes multiple on-chip resistors. For example, on-chip resistors 111, 121, 122, and 123 are shown in Figure 3. Each resistor network 101 can include any number of resistors. Four resistors are shown in Figure 3 merely as one example of the present invention.

[0024] Resistor network 101 also includes multiple pass gates. For example, pass gates 131, 132, 133, and 141 are shown in Figure 3. Each of pass gates 131-133 is coupled in series with one of resistors 121-123, as shown in Figure 3. Pass gate 141 is coupled in series with resistor 111 and resistors 121-123.

[0025] Pass gates 141 are controlled by control signals R[1:N] and complimentary signals RB[1:N], where N is the number of resistor networks 101 inside circuit 20. Thus, there are two voltage signals R and RB for each pass gate 141 in circuit 20. Signals R and RB are

programmed to select which of resistor networks 101 will be enabled to conduct current between terminals IN and CM.

[0026] Pass gates 141 and pass gates 131-133 can include two CMOS pass transistors (a p-channel FET and an n-channel FET) coupled in parallel. Voltage signals R control the n-channel transistors within each of the pass gates 141, and voltage signals RB control the p-channel transistors within each of the pass gates 141. According to further embodiments of the present invention, pass gates 141 and 131-133 each include only one pass transistor. In other embodiments, pass gates 141 and 131-133 each include three or more pass transistors.

[0027] For example, when signal R1 is HIGH, and signal RB1 is LOW, pass gate 141 in network 101-1 is ON. When signal R1 is LOW, and signal RBN is HIGH, pass gate 141 in network 101-1 is OFF.

[0028] Any of pass gates 141 can be turned ON to enable a corresponding one of resistor networks 101. When a pass gate 141 in a particular resistor network 101 is OFF, current flow through that resistor network 101 is blocked.

[0029] Pass gates 131-133 in each of resistor networks 101 are controlled by control signals C[1:M] and complimentary signals CB[1:M]. M is the total number of pass gates 131-133 within circuit 20. Voltage signals C control the n-channel transistors within pass gates 131-133, and voltage signals CB control the p-channel transistors within pass gates 131-133.

[0030] For example, when signal C1 is HIGH, and signal CB1 is LOW, pass gate 131 is network 101-1 is ON. When signal C1 is LOW, and signal CB1 is HIGH, pass gate 131 in network 101-1 is OFF. When signal C2 is HIGH, and signal CB2 is LOW, pass gate 132 is ON. When signal C2 is LOW, and signal CB2 is HIGH, pass gate 132 is OFF.

[0031] Any of pass gates 131-133 in circuit 20 (and any other pass gates) can be turned ON to couple a current path through resistors 121-123, respectively, using signals C and CB. For example, pass gate 133 can be turned ON to provide a current path through resistor 123 in one of networks 101. Any of pass gates 131-133 in circuit 20 can be turned OFF to block a current path through resistors 121-123, respectively, using signals C and CB. For example, pass gate 132 can be turned OFF to block current through resistor 122 in one of networks 101.

[0032] By turning ON pass gate 141 and one or more of pass gates 131-133 in one of resistor networks 101, a current path is opened up between terminals IN and CM in that

network 101. Current can flow through resistor 111 and one or more of resistors 121-123. A user of the integrated circuit can block current flow through any one of networks 101 in circuit 20 by turning OFF a corresponding one of pass gates 141.

[0033] Because resistor networks 101 are coupled in parallel with each other, the net resistance of circuit 20 can be reduced by turning ON more of pass gates 141. As current paths through more of networks 101 are opened up, the net resistance of circuit 20 decreases. Conversely, the net resistance of circuit 20 can be increased by turning OFF more of pass gates 141.

[0034] The net resistance of circuit 20 can also be reduced by turning ON more of pass gates 131-133, because resistors 121-123 are coupled together in parallel. Conversely, the net resistance of circuit 20 can be increased by turning OFF more of pass gates 131-133. The minimum resistance of circuit 20 can be achieved by turning ON all of the pass gates 141 and 131-133 in circuit 20 to provide the maximum number of current paths.

[0035] As user of the integrated circuit can control signals C, CB, R, and RB to set the net resistance of termination impedance circuit 20 to match the impedance of a transmission line. Pass gates 141 and 131-133 are turned ON or OFF to set the net resistance of circuit 20 to match the transmission line impedance.

[0036] One or more termination impedance circuits can be coupled to every IO pin on an integrated circuit, as shown for example, in Figures 1 and 2. Thus, the present invention provides techniques for setting the on-chip termination impedance to terminate transmission lines coupled to the IO pins. The net resistance of each circuit 20 can be programmed independently. Therefore, the on-chip termination impedance provided to each IO pin can be set to a different value to match each unique transmission line.

[0037] The present invention allows for real-time adjustment of on-chip termination impedance. For example, a user can build a feedback circuit based on an algorithm programmed into an integrated circuit. The feedback circuit can also take data from the transmission channel to determine whether the on-chip termination impedance is continuing to match the transmission line impedance. If the feedback circuit senses any changes in the on-chip termination impedance, the feedback circuit can dynamically adjust the on-chip termination impedance in real-time to compensate for these changes.

[0038] For example, as the temperature or the supply voltage of the integrated circuit changes, the resistance of resistors 111 and 121-123 also changes. Resistors 111 and 121-123 can be made, for example, of polysilicon. The feedback circuit senses the change in the termination impedance. The feedback circuit then causes or more pass gates 131-133 change state (i.e., turned ON or OFF) so that the net resistance of circuit 20 continues to match the transmission line impedance.

[0039] The feedback circuit generates control signals C, CB, R, and RB to dynamically adjust the on-chip termination impedance through gates 131-133 in circuit 20. These control signals also can be generated by other circuitry on the integrated circuit. For example, these control signals can be stored in a control RAM (CRAM) blocks on a field programmable gate array. These control signals can also be generated by programmable logic elements on a field programmable gate array. A user of the integrated circuit can program the logic elements and the CRAM blocks to generate the control signals that set the net resistance of termination impedance circuits 20. The logic elements and CRAM can be reprogrammed to change the net resistance of circuit 20. Alternatively, the user can set the values of signals C, CB, R, and RB through an input pin.

[0040] Pass gates 141 generally do not change state in response to temperature changes. Turning pass gates 141 ON or OFF causes larger changes in the net resistance of circuit 20, because gates 141 control current to several resistors. The changes caused by temperature and voltage variations are usually small. Smaller changes in the net resistance can be achieved merely by changing the state of one or more of pass gates 131-133. Therefore, the present invention provides techniques for dynamically compensating for variations in the resistances of on-chip termination resistors (caused by temperature changes, etc.) by controlling gates 131-133.

[0041] Further details of an exemplary field programmable gate array that can be used to implement the techniques of the present invention is now discussed. Figure 4 is a simplified partial block diagram of an exemplary high-density PLD/FPGA 400 that can be used to implement the present invention. PLD 400 includes a two-dimensional array of programmable logic array blocks (or LABs) 402 that are interconnected by a network of column and row interconnects of varying length and speed. LABs 402 include multiple (e.g., 10) logic elements (or LEs), an LE being a small unit of logic that provides for efficient implementation of user defined logic functions.

[0042] PLD 400 also includes a distributed memory structure including RAM blocks of varying sizes provided throughout the array. The RAM blocks include, for example, 512 bit blocks 404, 4K blocks 406 and a MegaBlock 408 providing 512K bits of RAM. These memory blocks may also include shift registers and FIFO buffers. PLD 400 further includes digital signal processing (DSP) blocks 410 that can implement, for example, multipliers with add or subtract features. I/O elements (IOEs) 412 located, in this example, around the periphery of the device support numerous single-ended and differential I/O standards. It is to be understood that PLD 400 is described herein for illustrative purposes only and that the present invention can be implemented in many different types of PLDs, FPGAs, and the like.

[0043] While PLDs of the type shown in figure 4 provide many of the resources required to implement system level solutions, the present invention can also benefit systems wherein a PLD is one of several components. Figure 5 shows a block diagram of an exemplary digital system 500, within which the present invention may be embodied. System 500 can be a programmed digital computer system, digital signal processing system, specialized digital switching network, or other processing system. Moreover, such systems may be designed for a wide variety of applications such as telecommunications systems, automotive systems, control systems, consumer electronics, personal computers, Internet communications and networking, and others. Further, system 500 may be provided on a single board, on multiple boards, or within multiple enclosures.

[0044] System 500 includes a processing unit 502, a memory unit 504 and an I/O unit 506 interconnected together by one or more buses. According to this exemplary embodiment, a programmable logic device (PLD) 508 is embedded in processing unit 502. PLD 508 may serve many different purposes within the system in Figure 5. PLD 508 can, for example, be a logical building block of processing unit 502, supporting its internal and external operations. PLD 508 is programmed to implement the logical functions necessary to carry on its particular role in system operation. PLD 508 may be specially coupled to memory 504 through connection 510 and to I/O unit 506 through connection 512.

[0045] Processing unit 502 may direct data to an appropriate system component for processing or storage, execute a program stored in memory 504 or receive and transmit data via I/O unit 506, or other similar function. Processing unit 502 can be a central processing unit (CPU), microprocessor, floating point coprocessor, graphics coprocessor, hardware controller, microcontroller, programmable logic device programmed for use as a controller,

network controller, and the like. Furthermore, in many embodiments, there is often no need for a CPU.

[0046] For example, instead of a CPU, one or more PLDs 508 can control the logical operations of the system. In an embodiment, PLD 508 acts as a reconfigurable processor, which can be reprogrammed as needed to handle a particular computing task. Alternately, programmable logic device 508 may itself include an embedded microprocessor. Memory unit 504 may be a random access memory (RAM), read only memory (ROM), fixed or flexible disk media, PC Card flash disk memory, tape, or any other storage means, or any combination of these storage means.

[0047] While the present invention has been described herein with reference to particular embodiments thereof, a latitude of modification, various changes, and substitutions are intended in the present invention. In some instances, features of the invention can be employed without a corresponding use of other features, without departing from the scope of the invention as set forth. Therefore, many modifications can be made to adapt a particular configuration or method disclosed, without departing from the essential scope and spirit of the present invention. It is intended that the invention not be limited to the particular embodiments disclosed, but that the invention will include all embodiments and equivalents falling within the scope of the claims.